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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,614	07/21/2000	Yasuyuki Morishita	040373/0287	4521
22428	7590	10/30/2003	EXAMINER	
FOLEY AND LARDNER SUITE 500 3000 K STREET NW WASHINGTON, DC 20007			NADAV, ORI	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 10/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/621,614

Applicant(s)

MORISHITA, YASUYUKI

Examiner

ori nadav

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Becerra et al. (5,710,689). APA teaches in figure 7 a semiconductor device having, on a semiconductor substrate 20, an input/output protection circuit section comprising a complementary N type field effect transistor wherein the complementary field effect transistor includes a first field effect transistor having source 3c and drain 3b diffusion layers of the first conductive type, respectively, and a gate electrode 6 that is disposed between these source and drain diffusion layers of the first conductivity type, and a second field effect transistor having source 4c and drain 4b diffusion layers of the second conductive type, respectively, and a gate electrode 5 that is disposed between these source and drain diffusion layers of the second conductivity type, wherein a source dopant diffusion region 4a of the second conductive type is set at a distance from the first field effect transistor, and a drain dopant diffusion region 3a of the first conductive type is set at a distance from the second field effect transistor,

an element isolation film 10 located in the substrate between the dopant diffusion region and the source diffusion layer of the first conductivity type for separating the dopant diffusion region from the source diffusion layer,

wherein the drain dopant diffusion region 4a is connected to a first reference potential V_{ss} , the drain dopant diffusion region 3a is connected to a second reference potential V_{dd} , and the drain diffusion layer 3b and the drain diffusion layer 4b of the first and second field effect transistors, respectively, are each connected directly to an input/output terminal section 7 without an intervening resistance element, and wherein the source diffusion layer of the first field effect transistor is connected to a constant ground terminal 9 and not connected to an input/output terminal section..

APA does not teach a first conductive type well under the first source diffusion layer and at least partially underlies the element isolation film, and having a lower dopant concentration than the first diffusion layer.

Becerra et al. teach in figure 4 a first conductive type well (n-well) under the first source diffusion layer (n+) and at least partially underlies the element isolation film (FOX region), and having a lower dopant concentration than the first diffusion layer, wherein the bottom of the first conductive type well is at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer in APA's device in order to provide

better electrical isolation to the device by forming the transistor in an n-well. Note that the broad recitation of the claim does not preclude the n-well from being located under the entire device..

Regarding claim 1, APA teaches in figures 14-15 and related text that an input/output protection circuit generally composed of a plurality of field effect transistors connected in parallel, each of which has source and drain diffusion layers of the first conductive type.

Regarding claims 2, 5 and 6, APA teaches a gate electrode of the first field effect transistor and the source dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom of the first conductive type well at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well in APA's device in order to increase the distance that a spike can propagate without shorting out the junction.

Regarding claim 6, APA teaches a dopant high-concentration region 20 beneath the second conductive type well, and containing second conductive type dopants with a higher dopant concentration than the second conductive type well.

Response to Arguments

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.
October 28, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800